$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or
$$I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA}$$

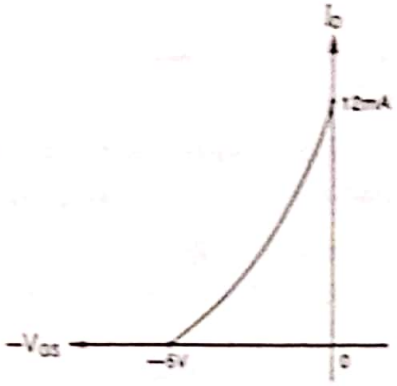


Fig. 21.14

Example 21.2. *A JFET has the following parameters:* $I_{DSS} = 32mA$; $V_{GS(off)} = -8V$; $V_{GS} = -4.5V$. *Find the value of drain current.*

Solution

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{mA}$$

$$= \mathbf{6.12\ mA}$$

Example 21.3. *A JFET has a drain current of 5mA. If* $I_{DSS} = 10mA$ *and* $V_{GS(off)} = -6V$, *find the value of (i)* V_{GS} *and (ii)* V_P.

Solution

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or
$$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$

or
$$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

$$\therefore \quad V_{GS} = \mathbf{-1.76V}$$

and
$$V_P = -V_{GS\,(off)} = \mathbf{6V}$$

21.11. Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(i) It has a very high input impedance (of the order of 100MΩ). This permits high degree of isolation between the input and output circuits.

(ii) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(iii) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runway.

(iv) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(v) A *JFET* has a smaller size, longer life and high efficiency.

21.12. Parameters of JFET

Like vacuum tubes, a *JFET* has certain parameters which determine its performance in a circuit. The main parameters of a *JFET* are *(i)* a.c. drain resistance *(ii)* transconductance *(iii)* amplification factor.

(i) **a.c. drain resistance** (r_d). Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a *JFET*. It may be defined as follows :

It is the ratio of change in drain-source voltage (ΔV_{DS}) *to the change in drain current* (ΔI_D) *at constant gate-source voltage i.e.*

$$\text{a.c. drain resistance } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of $2V$ produces a change in drain current of $0.02mA$, then

$$\text{a.c. drain resistance, } r_d = \frac{2\text{V}}{0.02\text{mA}} = 100\text{k}\Omega$$

Referring to the output characteristics of a *JFET* in Fig. 21.8, it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat. Therefore, drain resistance of a *JFET* has a large value, ranging from 10kΩ to 1MΩ.

(ii) **Transconductance** (g_{fs}). The control that the gate voltage has over the drain current is measured by transconductance g_{fs} and is similar to the transconductance g_m of the tube. It may be defined as follows :

It is the ratio of change in drain current (ΔI_D) *to the change in gate-source voltage* (ΔV_{GS}) *at constant drain-source voltage i.e.*

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a *JFET* is usually expressed either in mA/volt or micromhos. As an example, if a change in gate voltage of 0.1V causes a change in drain current of 0.3mA, then,

$$\text{Transconductance, } g_{fs} = \frac{0.3\text{mA}}{0.1\text{V}} = 3\text{mA/V} = 3 \times 10^{-3} \text{ A/V or mho}$$

$$= 3 \times 10^{-3} \times 10^{6} \,\mu\text{mhos} = 3000 \,\mu\text{mhos}$$

(iii) **Amplification factor** (μ).It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current *i.e.*

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a *JFET* indicates how much more control the gate voltage has over drain current than has the drain voltage. For instance, if the amplification factor of a *JFET* is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

21.13. Relation Among JFET Parameters

The relationship among *JFET* parameters can be established as under :

We know $$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$\Delta I_D = 10.25 - 9.65 = 0.6mA$$

$$\therefore \quad \text{Transconductance,} \quad g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.6mA}{0.2V} = 3mA/V = \mathbf{3000\ \mu mho}$$

(iii) Amplification factor, $\mu = (32 \times 10^3) \times (3000 \times 10^{-6}) = 96$

21.14. JFET Biasing

For the proper operation of *JFET*, gate must be negative *w.r.t.* source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit. The latter method is preferred because batteries are costly and require frequent replacement.

1. Bias battery. Fig. 21.15 shows the biasing of a *JFET* by a bias battery V_{GG}. This battery ensures that gate is always negative *w.r.t.* source during all parts of the signal.

2. Biasing circuit. The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are *(i)* self-bias *(ii)* potential divider method.

(i) **Self-bias.** Fig. 21.16 shows the self-bias method. The resistor R_S is the bias resistor. The d.c. component of drain current flowing through R_S produces the desired bias voltage. The capacitor C_S bypasses the a.c. component of the drain current.

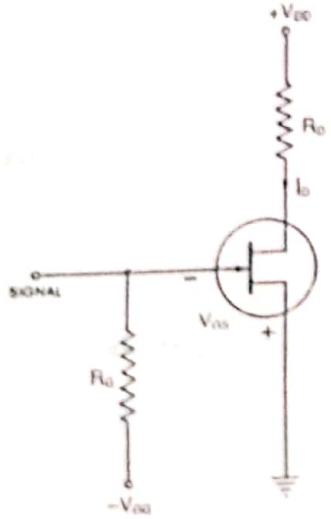


Fig. 21.15

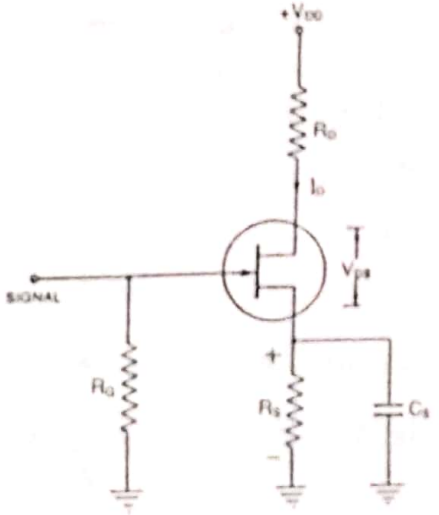


Fig. 21.16

Voltage across R_S, $\quad V_S = I_D R_S$

Since gate current is negligibly small, the gate terminal is at d.c. ground *i.e.*, $V_G = 0$

$$\therefore \quad V_{GS} = V_G - V_S = 0 - I_D R_S$$

or $$V_{GS} = -I_D R_S$$

Thus bias voltage V_{GS} keeps gate negative *w.r.t.* source.

Operating point. The operating point (*i.e.*, zero signal I_D and V_{DS}) can be easily determined. Since the parameters of the *JFET* are usually known, zero signal I_D can be calculated from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Also $$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Thus d.c. conditions of *JFET* amplifier are fully specified.

(ii) **Potential divider method.** Fig. 21.17 shows potential divider method of biasing a *JFET*. This circuit is identical to that used for a transistor. The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 across R_2 provides the necessary bias.

$$V_2 = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $$V_2 = V_{GS} + I_D R_S$$

or $$V_{GS} = V_2 - I_D R_S$$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under:

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

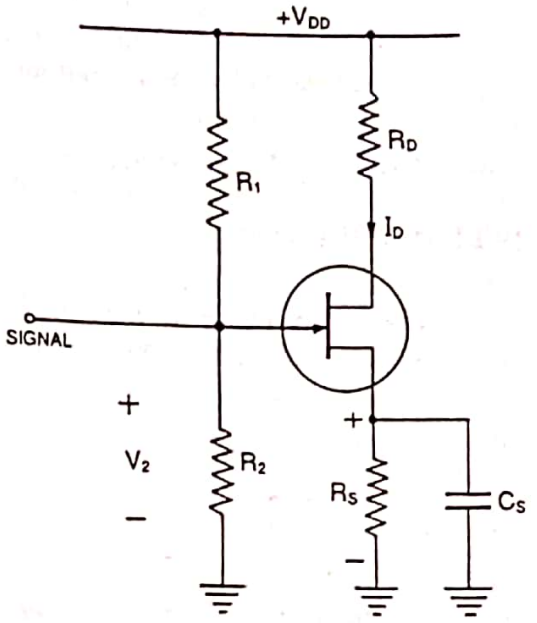


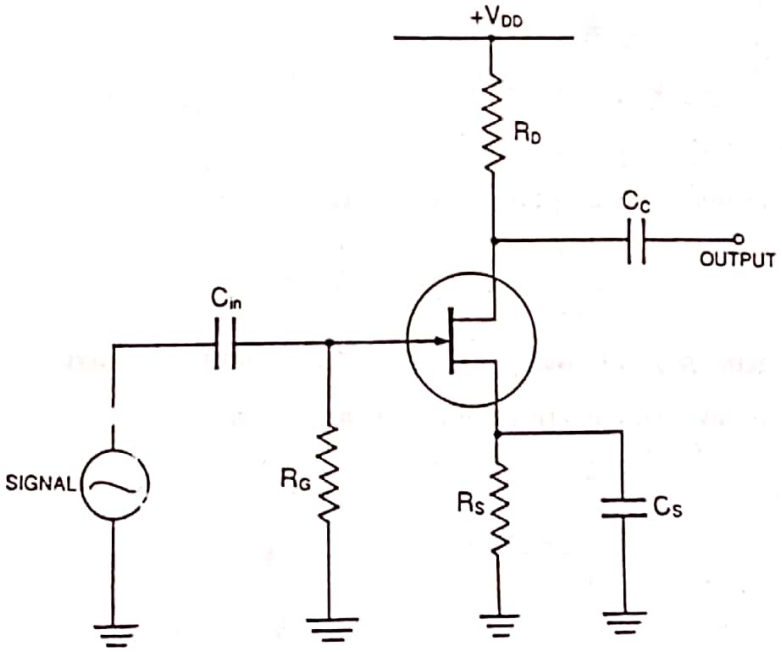
Fig. 21.17

21.15. JFET Connections

There are three leads in a *JFET viz.*, source, gate and drain terminals. However, when *JFET* is to be connected in a circuit, we require four terminals ; two for the input and two for the output. This difficulty is overcome by making one terminal of the *JFET* common to both input and output terminals. Accordingly, a *JFET* can be connected in a circuit in the following three ways :

(i) Common source connection *(ii)* Common gate connection

(iii) Common drain connection



Common source connection

Fig. 21.18

The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and a moderate output impedance. However, the circuit produces a phase reversal *i.e,.* output signal is 180° out of phase with the input signal. Fig. 21.18 shows a common source *n*-channel *JFET* amplifier. Note that source terminal is common to both input and output.

Note. A common source *JFET* amplifier is the *JFET* equivalent of common emitter amplifier. Both amplifiers have a 180° phase shift from input to output. Although the two amplifiers serve the same basic purpose, the means by which they operate are quite different.

Example 21.7. *In a self-bias n-channel JFET, the operating point is to be set at* $I_D = 1.5mA$ *and* $V_{DS} = 10V$. *The JFET parameters are* $I_{DSS} = 5mA$, *and* $V_P = -2V$. *Find the values of* R_S *and* R_D. *Given that* $V_{DD} = 20V$.

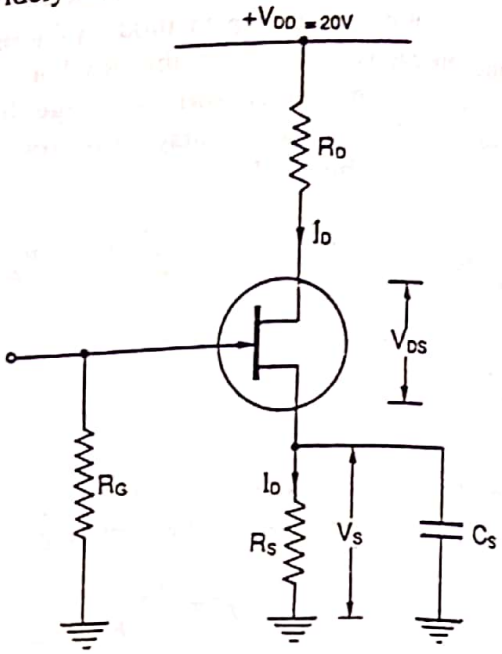


Fig. 21.19

Solution

Fig. 21.19 shows the circuit arrangement.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or $$1.5 = 5\left(1 + \frac{V_{GS}}{2}\right)^2$$

or $$1 + \frac{V_{GS}}{2} = \sqrt{1.5/5} = 0.55$$

or $$V_{GS} = -0.9V$$

Now, $$V_{GS} = V_G - V_S$$

or $$V_S = V_G - V_{GS}$$

$$= 0 - (-0.9) = 0.9V$$

$$\therefore \quad R_S = \frac{V_S}{I_D} = \frac{0.9V}{1.5mA} = \mathbf{0.6\ K\Omega}$$

Applying Kirchhoff's voltage law to the drain circuit, we have,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or $$20 = 1.5mA \times R_D + 10 + 0.9$$

$$\therefore \quad R_D = \frac{(20 - 10 - 0.9)V}{1.5mA} = 6\ K\Omega$$

Example 21.8. *In an n-channel JFET biased by potential divider method, it is desired to set the operating point at* $I_D = 2.5mA$ *and* $V_{DS} = 8V$. *If* $V_{DD} = 30V$, $R_1 = 1M\Omega$ and $R_2 = 500\ K\Omega$, *find the value of* R_S. *The parameters of JFET are* $I_{DSS} = 10mA$ *and* $V_P = -5V$.

Solution

Fig. 21.20 shows the conditions of the problem.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or $$2.5 = 10\left(1 + \frac{V_{GS}}{5}\right)^2$$

or $$1 + \frac{V_{GS}}{5} = \sqrt{2.5/10} = 0.5$$

or $$V_{GS} = -2.5V$$

Now, $$V_2 = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{30}{1000 + 500} \times 500 = 10V$$

$$V_2 = V_{GS} + I_D R_S$$

or $$10V = -2.5V + 2.5mA \times R_S$$

$$\therefore \quad R_S = \frac{10V + 2.5V}{2.5mA} = \frac{12.5V}{2.5mA} = 5\ \text{K}\Omega$$

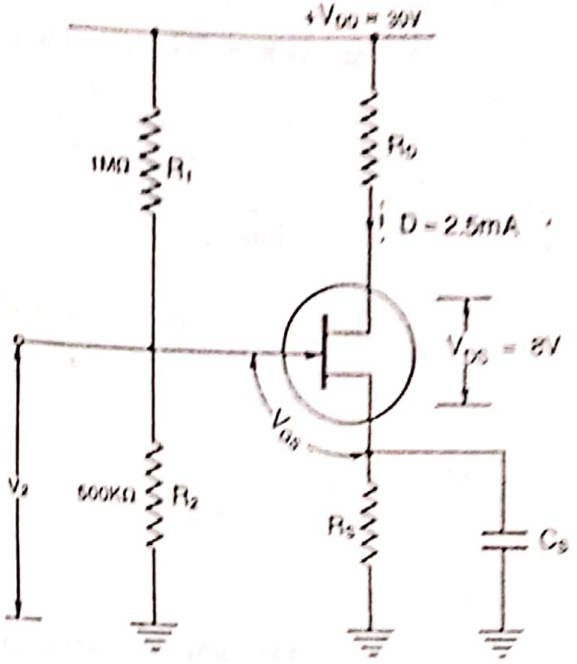


Fig. 21.20

21.16. Voltage Gain of JFET Amplifier

Fig. 21.21 shows a typical circuit of a *JFET* amplifier. The *JFET* is self-biased by using the biasing network $R_S - C_S$. The d. c. component of the drain current flowing through the source-biasing resistance R_S produces the desired bias voltage. The capacitor C_S bypasses the a.c. component of drain current. It may be noted that biasing circuit is similar to the cathode bias for a vacuum tube. The value of R_S can be determined from the following relation :

$$R_S = \frac{V_{GS}}{I_D}$$

where V_{GS} = voltage drop across R_S and I_D = current through R_S

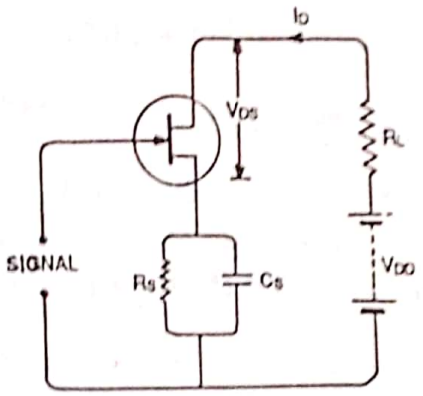


Fig. 21.21

Like a vacuum tube, a *JFET* is a voltage driven device. Therefore, the voltage gain of a *JFET* amplifier can be determined in the same manner as for a vacuum tube.

∴ Voltage gain of *JFET* amplifier,

$$A_v = \frac{\mu R_L}{r_d + R_L}$$

$$\text{Since } \mu = r_d \times g_{fs} \qquad \therefore \quad A_v = \frac{r_d\, g_{fs}\, R_L}{r_d + R_L}$$

If $r_d >> R_L$, then the latter can be neglected as compared to the former.

$$\therefore \qquad \text{Voltage gain, } A_v = \frac{r_d\, g_{fs}\, R_L}{r_d} \text{ or } \qquad A_v = g_{fs} \times R_L$$

Example 21.9. *The transconductance of a JFET used in a voltage-amplifier circuit is 3000 μmhos and the load resistance is 10 kΩ. Calculate the voltage amplification of the circuit assuming that $r_d >> R_L$.*

Solution.

$$g_{fs} = 3000\ \mu mhos = 3000 \times 10^{-6}\ mho \qquad \text{and} \qquad R_L = 10\ k\Omega = 10{,}000\ \Omega$$

As $r_d >> R_L$,

$$\therefore \qquad A_v = g_{fs} R_L = (3000 \times 10^{-6}) \times (10{,}000) = \mathbf{30}$$

Example 21.10 *In the JFET circuit shown in Fig 21.22, find (i) V_{DS} and (ii) V_{GS}.*

Solution.

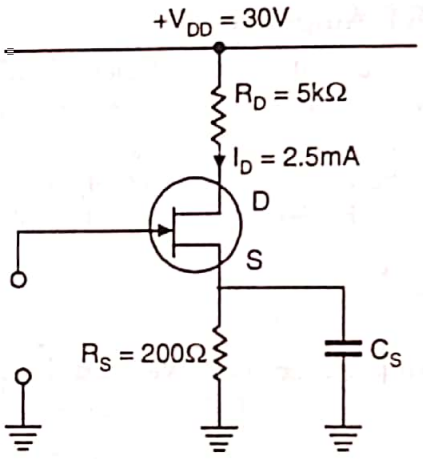


Fig. 21.22

$$V_{DS} = V_{DD} - I_D\,(R_D + R_S) = 30 - 2.5\text{mA}\,(5 + 0.2) = 30 - 13 = \mathbf{17V}$$

$$V_{GS} = -I_D R_S = -(2.5 \times 10^{-3}) \times 200 = \mathbf{-0.5V}$$

Example 21.11. *Figure 21.23 shows two stages of JFET amplifier. The first stage has I_D = 2.15mA and the second stage has I_D = 9.15mA. Find the d.c. voltage of drain and source of each stage w.r.t. ground.*

Solution

Voltage drop in 8.2kΩ

$$= 2.15\text{mA} \times 8.2\text{k}\Omega = 17.63\text{V}$$

D.C. Potential of drain of first stage *w.r.t.* ground

$$V_D = V_{DD} - 17.63 = 30 - 17.63 = \mathbf{12.37V}$$

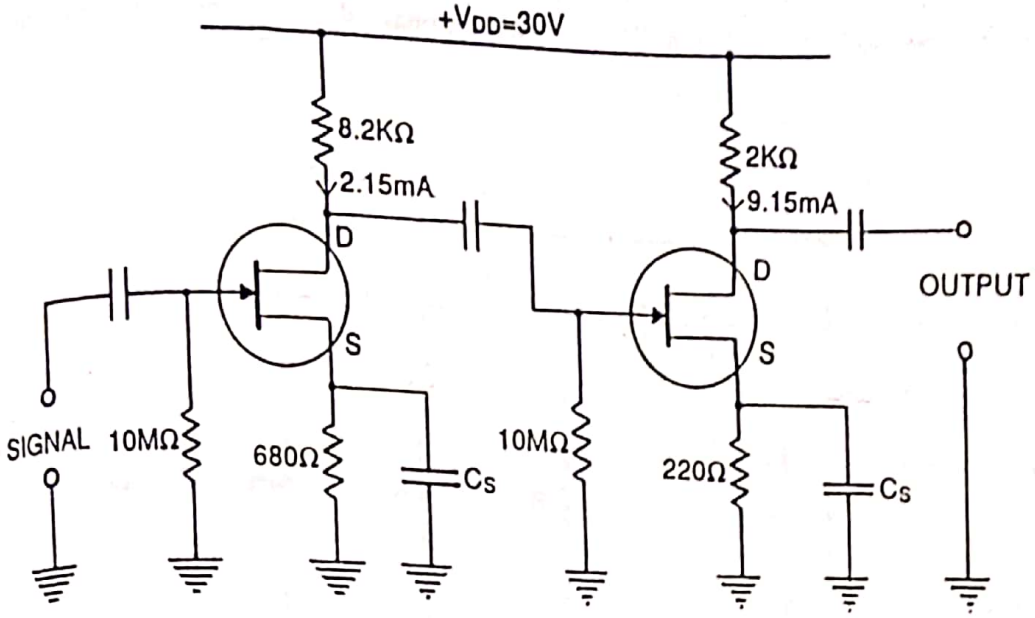


Fig. 21.23

D.C. potential of source of first stage to ground

$$V_S = I_D R_S = 2.15mA \times 0.68K\Omega = \mathbf{1.46V}$$

Voltage drop in $2K\Omega = 9.15mA \times 2K\Omega = 18.3V$

D.C. potential of drain of second stage to ground

$$V_D = V_{DD} - 18.3 = 30 - 18.3 = \mathbf{11.7V}$$

D.C. Potential of source of second stage to ground

$$V_S = I_D R_S = 9.15\text{mA} \times 0.22K\Omega = \mathbf{2.01V}$$

21.17. JFET Applications

The high input impedance and low output impedance and low noise level make *JFET* far superior to the bipolar transistor. Some of the circuit applications of *JFET* are :

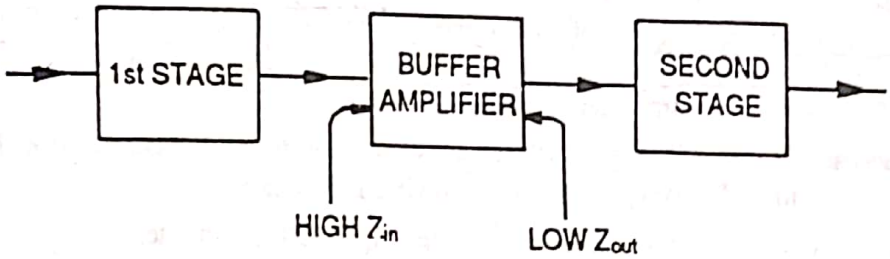


Fig. 21.24

(i) **As a buffer amplifier.** A buffer amplifier is a stage of amplification that isolates the preceding stage from the following stage. Because of the high input impedance and low output impedance, a *JFET* can act as an excellent buffer amplifier (See Fig. 21.24). The high input impedance of *JFET* means light loading of the preceding stage. This permits almost the entire output from first stage to appear at the buffer input. The low output impedance of *JFET* can drive heavy loads (or small load resistances). This ensures that all the output from the buffer reaches the input of the second stage.